UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,646	09/17/2003	Yutaka Ohmoto	500.39750VX1	3794

20457 7590 09/08/2005

ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-3873

EXAMINER	
DHINGRA, RAKESH KUMAR	
ART UNIT	**PAPER NUMBER**
1763	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,646	OHMOTO ET AL.	
	Examiner	Art Unit	
	Rakesh K. Dhingra	1763	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/17/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/17/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/795,487.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/03, 3/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Specification

The disclosure is objected to because of the following informalities:

Figure 7: Reference number 23A is not described in the specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 2, 3, 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masuda et al (US Pub. No. 2002/0005252) in view of Seiichi et al (JP Pub. No. 08-316212).

Regarding Claims 1, 2, 5: Masuda et al teach a plasma processing apparatus (Figure 1) for manufacturing a semiconductor device comprising:

A process chamber 100 with means 122, 141 for applying high frequency into the chamber, means 117 for process gas supply, electrode system 130 with chuck (mounting table) 131 for mounting substrate W;

means 141 for applying bias powers to a substrate W to be processed and

a sample holder ring (material) 132 adjacent to said substrate and having means for adjusting a feeding impedance for the bias power applied to said material (Paragraphs 0047, 0049, 0052, 0055); Masuda et al further teach that by leaking and adding a part of bias power from the bias power source 141 to sample holder ring 132 via insulator 133, it is possible to adjust the application of bias power to ring 132 (Column 0055).

Masuda et al do not teach means for adjusting feeding impedance for bias powers to a plurality of positions on the substrate.

Seiichi et al teach a plasma processing apparatus (Figures 1-7) comprising impedance adjusting means 11 (Figure 4) for the bias powers for different positions in said substrate differently so as to make uniform plasma (Paragraphs 0008, 0009, 0010). Seiichi et al further teach that by dividing the substrate area into plural parts the impedance can be adjusted to enable uniform plasma treatment over the surface of the substrate.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use impedance changing means as taught by Seiichi et al in the apparatus of Masuda et al to carry out more uniform plasma treatment.

Regarding Claim 3: Seiichi et al teach that by changing ratio of capacity of variable capacitors 13 in Figure 13 (impedance matching means) the ratio of high

frequency power supplied to different sections of the substrate can be changed and more uniform plasma treatment can be achieved (Paragraphs 0008).

Claims 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masuda et al (US Pub. No. 2002/0005252) in view of Seiichi et al (JP Pub. No. 08-316212) as applied to Claims 1, 2, 5 and further in view of Hao et al (US Patent No. 6,363,882) and Shamouillian et al (US Patent No. 6,557,248).

Regarding Claim 4: Masuda et al in view of Seiichi et al teach all limitations of the claim including that thickness and material of the insulator 133 can be used to adjust the bias power to be applied to the ring 132 (Masuda et al, Paragraph 0066).

Masuda et al in view of Seiichi et al do not teach insulating layer between electrode and substrate, plurality of insulating layers and conducting material in insulating layer.

Hao et al teach an apparatus (Figure 3) that has an impedance matching layer (insulating layer) 158 that is configured for controlling the impedance of electric field produced by electrode 152 (conductive material) across the surface of the substrate. Hao et al further teach that the impedance matching layer can be coupled to upper surface of electrode 152 or coupled to lower surface of edge ring 156 (Column 6, lines 40-67).

Further Shamouillian et al teach an electrostatic chuck (Figure 1a) 20 that has plurality of insulating layers 35a, 35b, an upper surface 40 for receiving substrate 45 thereon and with an electrode 50 (conductive material) within the insulating

layer that is connected to voltage supply terminal 70 and the chuck is electrically biased by power supply 85 (Column 5, lines 1-13 and lines 55-60).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use insulating layers (impedance matching layers) as taught by Hao et al and Shamouillian et a in the apparatus of Masuda et al in view of Seiichi et al to obtain impedance adjusting means for the substrate and the material.

Claims 6-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masuda et al (US Pub. No. 2002/0005252) in view of Seiichi et al (JP Pub. No. 08-316212), Hao et al (US Patent No. 6,363,882) and Shamouillian et al (US Patent No. 6,557,248) and further in view of Kholodenko et al (US Patent No. 5,942,039).

Regarding Claims 6- 9, 11: Masuda et al in view of Seiichi et al, Hao et al and Shamouillian et al teach all limitations of the claim including that thickness and material of the insulator 133 can be used to adjust the bias power to be applied to the ring 132 (Masuda et al, Paragraph 0066) as discussed above.

Masuda et al in view of Seiichi et al, Hao et al and Shamouillian et al do not teach conducting material in the insulating layer of the material.

Kholodenko et al teach an apparatus (Figure 1) that has a focus ring 90 around wafer 25 and has an electrical conductor element 100 that is disposed within insulator 92 and is electrically connected to electrode 65a and is thus electrically biased with respect to other electrode 65b (Column 3, lines 63-67, Column 4, lines 10-20, and Column 5, lines 35-45).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have conductive material in the insulating layer of the material as taught by Kholodenko et al in the apparatus of Masuda et al in view of Seiichi et al, Hao et al and Shamouillian et al to reduce deposition of sputter-of deposits from the surface of focus ring (Column 4, lines 1-3).

Regarding Claim 10: Kholodenko et al teach that the apparatus of the invention can be used for semiconductor processes like CVD, etching (Column 7, lines 60-65) which would therefore inherently use semiconductor wafer. Kholodenko et al further teach that the conductor element 100 (member) adjacent to wafer is an electrical conductor (Column 3, lines 63-67).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Ohmi et al (US Patent No. 6,719,875) teach an apparatus (Figure 15) that has an auxiliary electrode 1503 adjacent to wafer 1509 and connected to high frequency power sources 1506, 1505 through impedance matching circuits 1508, 1507 respectively.

Yokogawa et al (US Pub. No. 2002/0020494) teach an apparatus (Figure 1) that has a ring shaped member 12 with silicon film 13 and arranged on the periphery of sample 6. A capacitor 14 divides the bias applied to sample 6 to apply resultant bias to silicon film 13.

Kikuchi et al (US Pub. No. 2004/0177927) teach an apparatus (Figure 1) that has a focus ring 9 surrounding a wafer W and a DC voltage application unit 30 for controlling electrical potential of the focus ring and lower electrode 4 is connected to high frequency power supply 32 via a matching circuit 31.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rakesh K. Dhingra whose telephone number is (571)-272-5959. The examiner can normally be reached on 8:30 -6:00 (Monday - Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Parviz Hassanzadeh can be reached on (571)-272-1435. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Rakesh Dhingra

Parviz Hassanzadeh
Supervisory Patent Examiner
Art Unit 1763